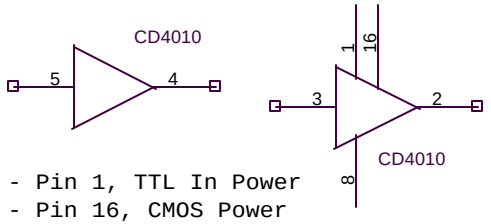
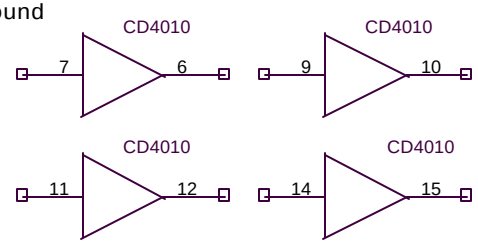
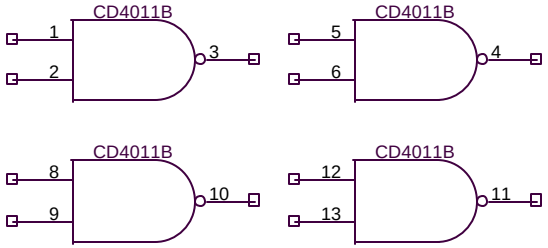



VCC - Pin 1, TTL In Power
VDD - Pin 16, CMOS Power
VSS - Pin 8, Common Ground

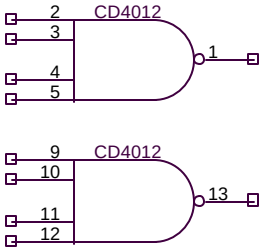



CD4010 TTL to CMOS Non-Inverting Buffer




VDD - Pin 14 (+3 to +15 V)
VSS - Pin 7 (Ground)

CD4011 Quad 2-Input NAND Gate




VDD - Pin 14 (+3 to +15 V)
VSS - Pin 7 (Ground)

CD4012 Dual 4-Input NAND Gate

| | | |
|---|---|---|
| Title: CMOS Class | | |
| Size: A | Document Number: Design 72 | Rev: 1 |
| Date: Tuesday, March 20, 2007 | Sheet 2 of 2 | |